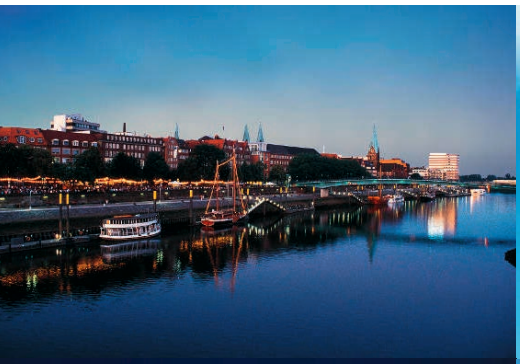
PATMOS & VARI 2016



Program Book

Bremen, 21–23 September

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PATMOS & VARI 2016
Editor: Kerstin Janssen
Layout & Cover: Janine Biermann, Universität Bremen
Print: Universität Bremen
Pictures: BTZ Bremer Touristik-Zentrale

Alberto García-Ortiz

Domenik Helms

Antonio Rubio Sola

Dear participants,

Welcome to Bremen, it is our great pleasure to invite you to join our unique event. During two weeks in September, Bremen is holding five international conferences focusing on hardware design. PATMOS and VARI are the closing conferences of this important series of research conferences.

PATMOS is one of the first conferences world-wide to focus on low power, with highest standards in vision and research quality. VARI is unique in Europe. It answers to the need to have a European event on variability in CMOS circuits and technologies to discuss the CMOS process for the design of integrated circuits and systems.

Science is based on interaction, and the informal and dynamic philosophies of PATMOS and VARI have been key ingredients for boosting this scientific interaction. We have created a number of opportunities for you to exchange ideas beyond the scientific schedule.

Despite having doubled the number of gray hair, it has truly been a pleasure to work with friends on this project. Recognition should go to the TPC and to the Local Organizers, who have all worked extremely hard. Our special thanks go to Jorge Juan, Nadine Azemard, Josep L. Rosselló, and all the persons alongside the organizing team that contributed to make PATMOS and VARI a success.

We very much hope that you will enjoy these two conferences and your stay in Bremen.

General Chairs PATMOS
Alberto García-Ortiz
Domenik Helms,

General Chairs VARI
Alberto García-Ortiz
Antonio Rubio Sola

Aida Todri-Sanial

Ricardo Reis

Steffen Paul

Gilles Jacquemod

Dear colleagues,

It is with great pleasure to welcome you to the IEEE PATMOS 2016 and the IEEE VARI 2016.

PATMOS is bringing together leading scientists and researchers from academia and industry. Top selected papers will be also encouraged to be part of a special issue on Integration, The VLSI Journal. This year we had 44 submissions and accepted 15 regular papers with a 34% acceptance rate. Additionally, we have organized 4 special sessions on most interesting topics. As a novelty, we have introduced a session related to on-going European projects related to ICT. It is a particular pleasure to present our two excellent keynote speakers, Prof. Asen Asenov and Prof. Christian Piguet and we celebrate the contribution of Prof. Piguet to the PATMOS community.

As is now a fruitful tradition, VARI and PATMOS are collocated. Today low-power, variability and reliability are closely connected with growing importance. These topics influence the whole design process. Prof.Tibor Grasser gives a keynote on Time-Dependent Variability in Scaled MOS-Transistors. Dr. Christian Schlünder from Infineon Technologies presents first hand industrial experience in his tutorial Variability and Reliability trouble in Semiconductor Product Design. Scientific contributions discuss new ideas on modeling, robust circuit design, and monitoring of process variations as well as aging.

We wish you a very productive workshop and hope you will find these proceedings to be a valuable reference for your future work.

Program Chairs PATMOS
Aida Todri-Sanial
Ricardo Reis

Program Chairs VARI
Steffen Paul
Gilles Jacquemod

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Alberto García-Ortiz, Universität Bremen, Germany
Domenik Helms, OFFIS, Germany

Program Chairs

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Aida Todri-Sanial, LIRMM, France

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PATMOS & VARI 2016
Tutorials & Invited

Wednesday – September 21st

Keynote

Design Technology Co-Optimisation in Advanced Technogogy Nodes

Prof. Asen Asenov, University of Glasgow, Scotland

Thursday – September 22nd

Keynote

Some Notes about the History of Low-Power

Prof. Chistian Piguet, CSEM, Switzerland

Thursday – September 22nd

Keynote

Time-dependent Variability in Scaled MOS-Transistors

Prof. Tibor Grasser, TU Wien, Austria

Thursday – September 22nd

VARI Tutorial

Variability and Reliability trouble Semiconductor Product Design

Dr. Christian Schlünder,
Infineon Technologies AG

Wednesday September 21, 2016

8:00 – 8:30	**Registration**
8:30 – 9:00	**Welcome note from General and Program Chairs**
9:00 – 10:00	Keynote **Design Technology Co-Optimization in Advanced Technology Nodes** *Prof. Asen Asenov, University of Glasgow, Scotland*
10:00 – 10:30	**Coffee Break**
10:30 – 11:45	PATMOS Session on **Power Reduction in Multi-core Systems** *Session chair: Ralph Görgen, OFFIS*
25 min	**Performance Estimation of Program Partitions on Multi-core Platforms** *Malgorzata Michalska, Junaid Jameel Ahmad, Endri Bezati, Simone Casale Brunet and Marco Mattavelli* *EPFL, Switzerland*
25 min	**Pipelining for Dual Supply Voltage** *Teng Xu and Miodrag Potkonjak* *University of California, Los Angeles, USA*
25 min	**Thermally-Aware Composite Run-Time CPU Power Models** *Matthew Walker[1], Stephan Diestelhorst[2], Andreas Hansson[2], Domenico Balsamo[2], Geoff Merrett[1] and Bashir Al-Hashimi[1]* *[1]University of Southampton, UK, [2]ARM Ltd., UK*
11:45 – 13:00	PATMOS Session on **Optimization of Thermal Management and Energy Efficiency in Nano-Electronic Devices and Systems** *Session Chair: T. Sadi, University of Glasgow*
25 min	**Investigation of Electro-Thermal Modeling and Analysis of Carbon Nanotube Interconnects** *Aida Todri-Sanial* *CNRS-LIRMM/University of Montpellier, France*

Wednesday September 21, 2016

	25 min	**Multi-Scale Electrothermal Simulation and Modeling of Resistive Random Access Memory Devices** *Toufik Sadi, Liping Wang, Asen Asenov,* *University of Glasgow, Scotland*
	25 min	**Thermoelectric Effects in Graphene and Graphene-Based Nanostructures using Atomistic Simulation** *Philippe Dollfus, Viet Hung Nguyen, Van Truong Tran, Mai Chung Nguyen, Arnaud Bournel, Jerome Saint-Martin* *CNRS/Université Paris Sud, Paris*
13:00 – 14:30		**Lunch**
14:30 – 16:00		PATMOS Session on **Near-Threshold Computing** *Session chair: M. Tahoori, KIT*
	22 min	**Fully Digital On-Chip Memory Using Minimum Height Standard Cells for Near-Threshold Voltage Computing** *Jun Shiomi, Tohru Ishihara, Hidetoshi Onodera* *Graduate School of Informatics, Kyoto University, Japan*
	22 min	**Hold-time Violation Analysis and Fixing in Near-Threshold Region** *Mohammad Saber Golanbari, Saman Kiamehr, Mehdi Tahori* *KIT, Germany*
	22 min	**Design Challenges for Near and Subthreshold Operation: A Case Study with an ARM Cortex-M0+ based WSN Subsystem** *James Myers, Pranay Prabhat, Anand Savanth, Sheng Yang, Rohan Gaddh* *ARM Ltd., Cambridge, UK*
	22 min	**Throughput Balancing for Energy Efficient Near-Threshold Manycores** *Ioannis Stamelakos[2], Sotirios Xydis[1], Gianluca Palermo[2], Cristina Silvano[2]* *[1]National Technical University of Athens, Greece* *[2]Politecnico di Milano, Italy*

16:00 – 16:45	Coffee Break and Poster Session

CMOS Process Transient Noise Simulation Analysis and Benchmarking
Thomas Noulis
Aristotle University of Thessaloniki, Greece

Secure Cryptographic Hardware Implementation Issues for High-Performance Applications
Erica Tena-Sánchez, Antonio José Acosta Jiménez and Juan Núnez Martínez.
Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla), Spain

Coarse-Grained Learning-Based Dynamic Voltage Frequency Scaling for Video Decoding
Jia Guo and Miodrag Potkonjak
University of California Los Angeles, USA

TransMem: A memory architecture to support dynamic Remapping and Parallelism in low power high performance CGRAs
Muhammad Adeel Tajammul, Syed Mohammad Asad Hassan Jafri, Ahmed Hemani and Peeter Ellerve
Royal Institute of Technology, Sweden

Deduplication in Resistive CAM Based SSD
Roman Kaplan, Leonid Yavits, Amir Morad and Ran Ginosar
Technion, Israel

Leakage Current Analysis in Static CMOS Logic Gates for a Transistor Network Design Approach
Jorge Tonfat, Guilherme Flach and Ricardo Reis
UFRGS, Brazil

Run-Time Schedulability Check of Real-Time Tasks for Energy Efficiency
Parham Haririan and Alberto Garcia-Ortiz
University of Bremen, Germany

Analysis of Stress Effects on Timing of nano-Scaled CMOS Digital Integrated Circuits
Hossein Aghababa, Mohammadreza Kolahdouz and Behjat Forouzandeh
University of Tehran, Iran

Thursday September 22, 2016

8:30 – 9:30		Keynote** **Some Notes about the History of Low-Power** *Prof. Christian Piguet, CSEM SA Neuchatel, Switzerland* **Celebrating Prof. Piguet's Career and Contribution to PATMOS
9:30 – 11:00		VARI Regular Session on **Variability and aging in the circuit design process** *Session chair: Prof. Steffen Paul, ITEM*
	25 min	**Design and Verification of Analog CMOS Circuits Using the gm/ID-Method with Age-Dependent Degradation Effects** *Theodor Hillebrand, Timur Schäfer, Nico Hellwege, Dagmar Peters-Drolshagen and Steffen Paul* *University of Bremen, Germany*
	25 min	**RRAM Variability and Its Mitigation Schemes** *Peyman Pouyan[1], Esteve Amat[1], Said Hamdioui[1] and Antonio Rubio[2]* *[1]TU Delft, Netherlands, [2]UPC, Spain*
	20 min	**A Framework for Analyzing the Propagation of Hardware-induced Errors in Linear Time-invariant Blocks with Finite Wordlength Effects** *Georgia Psychou, Tobias Gemmeke and Tobias G. Noll* *Imec, Belgium*
	20 min	**Investigating PVT Variability Effects on Full Adders** *Vinícius Zanandrea, Stéphanie Ames, Ingrid Oliveira, Samuel Toledo and Cristina Meinhardt* *Universidade Federal do Rio Grande, Brazil*
11:00 – 11:30		**Coffee Break**
11:30 – 12:30		Keynote **Time-Dependent Variability in Scaled MOS-Transistors** *Prof. Tibor Grasser, TU Wien, Austria*
12:30 – 14:00		**Lunch**

14:00 – 15:00 VARI Tutorial:
Variability and Reliability trouble Semiconductor Product Design
Dr. Christian Schlünder, Infineon Technologies AG

15:00 – 16:20 PATMOS Session on
European Projects

20 min **Project CONNECT**
Presenter: Aida Todri-Sanial, CNRS, France

20 min **Project SUPERAID7: Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7 nm node**
Presenter: Jürgen K. Lorenz, Fraunhofer IISB

20 min **Project nanoCOPS**
Presenter: Presenter: Jan ter Maten, University of Wuppertal

20 min **Project CLERECO: Cross-Layer Early Reliability Evaluation for the Computing continuum**
Presenter: Stefano Di Carlo - Politecnico di Torino

16:20 – 17:00 **Coffee Break and Poster Session**

Loop Optimization in Presence of STT-MRAM Caches: a Study of Performance-Energy Tradeoffs
Pierre-Yves Péneau[1], Rabab Bouziane[2], Abdoulaye Gamatie[1], Erven Rohou[2], Florent Bruguier[1], Gilles Sassatelli[1], Lionel Torres[1] and Sophiane Senni[1]
LIRMM, France, INRIA, France

Securing Embedded Systems and their IPs with Digital Reconfigurable PUFs
Jason Xin Zheng, Teng Xu and Miodrag Potkonjak
University of California Los Angeles, USA

Energy Efficiency of 2-Step Power-Clock for Adiabatic Logic
Himadri Singh Raghav, Vivian Bartlett and Izzet Kale
University of Westminster, UK

A Software Framework to Calculate Local Temperatures in CMOS Processors
Alireza Rohani, Hassan Ebrahimi and Hans Kerkhoff
University of Twente, Netherlands

Thursday September 22, 2016

	Subthreshold-Based m-Sequence Code Generator for Ultra Low-Power Body Sensor Nodes *Ahmad Abdulfattah, Charalampos Tsimenidis and Alex Yakovlev* *Newcastle University, UK*
	Novel Memristive Logic Architectures *Xiaohan Yang, Adedotun Adeyemo, Anu Bala and Abusaleh Jabir* *Oxford Brookes University, UK*
	Using Iddt Current Degradation to Monitor Ageing in CMOS Circuits *Radi Husin Ramlee and Mark Zwolinski*
	PMHLS 2.0: An Automated Optimization of Power Management During High-Level Synthesis *Dominik Macko* *Slovak University of Technology in Bratislava, Slovakia*
17:00 – 18:00	PATMOS Session on **Low-Power Design**
25 min	**Enabling Environmentally-Powered Indoor Sensor Networks With Dynamic Routing and Operation** *Jia Guo, Teng Xu, Theano Stavrinos and Miodrag Potkonjak* *University of California Los Angeles, USA*
25 min	**Automatic Design of Arbitrary-Size Approximate Sorting Networks with Error Guarantee** *Vojtech Mrazek and Zdenek Vasicek* *Brno University of Technology, Czech Republic*
19:40	**Meeting for Dinner** Location TBD
20:00	**Banquet Dinner – Jürgenshof**

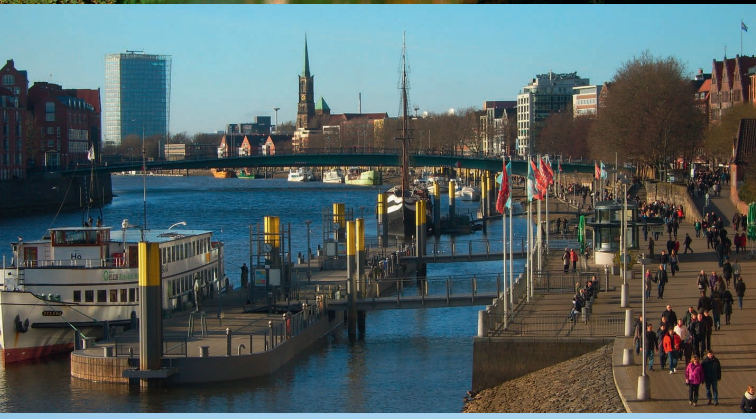
Friday September 23, 2016

08:30 – 10:00	PATMOS Session on **Design of Reliable and Energy Efficient Systems** *Session chair: Nils Koppaetzky, OFFIS*
25 min	**Comparison of Low-Voltage Scaling in Synchronous and Asynchronous FD-SOI Circuits** *Thiago Ferreira de Paiva Leite, Rodrigo Possamai Bastos, Rodrigo Iga and Laurent Fesquet* *Univ. Grenoble Alpes, CNRS, TIMA, Grenoble, France*
25 min	**Green Metadata Based Adaptive DVFS for Energy Efficient Video Decoding** *Yahia Benmoussa[1], Eric Senn[1], Nicolas Derouineau[2], Niclas Tizon[2], and Jalil Boukhobza[3]* *[1]Universite de Bretagne Sud, France, [2]Vitec, France, [3]Universite de Bretagne Occidentale, France*
25 min	**Pushing Minimum Energy Limits by Optimal Asymmetrical Back Plane Biasing in 28 nm UTBB FD-SOI** *Francisco Veirano[1], Lirida Naviner[2] and Fernando Silveira[1]* *[1]Universidad de la República, Uruguay,* *[2]Telecom ParisTech, France*
10:00 – 10:30	**Coffee Break**
10:30 – 12:00	PATMOS Session on **Modeling and Simulation of Emerging Devices and Interconnects** *Session chair: Domenik Helms, OFFIS*
25 min	**Physical Description and Analysis of Doped Carbon Nanotube Interconnects** *Jie Liang, Liuyang Zhang, Nadine Azemard-Crestani, Pascal Nouet, Aida Todri-Sanial* *CNRS-LIRMM/University of Montpellier France*
25 min	**Impact of Pipeline in the Power Performance of Tunnel Transistor Circuits** *María J. Avedillo and Juan Núñez* *Instituto de Microelectrónica de Sevilla, IMSE-CNM CSIC/Universidad de Sevilla, Spain*

Friday September 23, 2016

	25 min	**Energy Modeling of Coupled Interconnects including Misalignment Effects** *Amir Najafi, Ardalan Najafi, Ayad Dalloo and Alberto García-Ortiz* *ITEM, Univerity of Bremen, Germany*
	10 min	**A Novel Leakage Power Reduction Technique for Nano-Scaled CMOS Digital Integrated Circuits** *Hossein Aghababa, Mohammadreza Kolahdouz and Behjat Forouzandeh* *University of Tehran, Iran*
12:00 – 13:30		**Lunch**
13:30 – 15:00		PATMOS Session on **Power Aware Heterogeneous MPSoC – Memory & NoC Optimization** *Session Organizers: Jürgen Becker, Peter Figuli, Falco Bapp, KIT, Germany*
	22 min	**Energy Profile Analysis of Zynq-7000 Programmable SoC for Embedded Medical Processing: Case study on ECG Arrhythmia Detection** *Konstantinos Railis, Vasileios Tsoutsouras, Sotirios Xydis, Dimitrios Soudris* *TU Athens, Greece*
	22 min	**A New Bank Sensitive DRAM Power Model for Efficient Design Space Exploration** *Matthias Jung, Deepak M. Mathew, Eder F. Zulian, Christian Weis, Norbert Wehn* *TU Kaiserslautern, Germany*
	22 min	**The Long Way to Power Efficient, High Performance DRAMs** *Klaus Hofmann* *TU Darmstadt, Germany*
	22 min	**Document Classification Systems in Heterogeneous Computing Environments** *Nasibeh Nasiri[1], Philip Colangelo[1], Oren Segal[1], Martin Margala[1], Wim Vanderbauwhede[2]* *[1]UMASS, USA* *[2]University of Glasgow, UK*

15:00 – 16:30	PATMOS Session on **European Projects** *Session Chair: Domenik Helms, OFFIS, Germany*
22 min	**Project: BASTION Board and SoC Test Instrumentation for Ageing and No Failure Found** *Presenter: Artur Jutman, Testonica, Estonia*
22 min	**Project MoRV: Modelling Reliability under Variability** *Presenter: Nils Koppaetzky, OFFIS, Germany*
22 min	**Project ARGO: WCET-Aware Parallelization of Model-Based Applications for Heterogeneous Parallel Systems** *Presenter: Harald Buchner, KIT, Germany*
22 min	**Project Contrex: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties** *Presenter: Ralph Görgen, OFFIS, Germany*
16:30 – 17:20	PATMOS Special Session on **Optimization of Thermal Management and Energy Efficiency in Nano-Electronic Devices and Systems** *Session Chair: T. Sadi, University of Glasgow*
25 min	**Multiscale Modeling of Electron-Ion Interactions for Engineering Novel Electronic Devices and Materials** *Luca Larcher, Francesco Puglisi, Andrea Padovani, Luca Vandelli, Paolo Pavan, Universita di Modena e Reggio Emilia, Italy*
25 min	**Optimized Few Layer Graphene for Heat Spreading** *Sebastian Volz, Haoxue Han* *EM2C/ Ecole Centrale Paris, France*
17:20 – 18:00	**Closing & Award Ceremony** **Refreshment**




KUNSTHALLE BREMEN
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KUNSTHALLE BREMEN

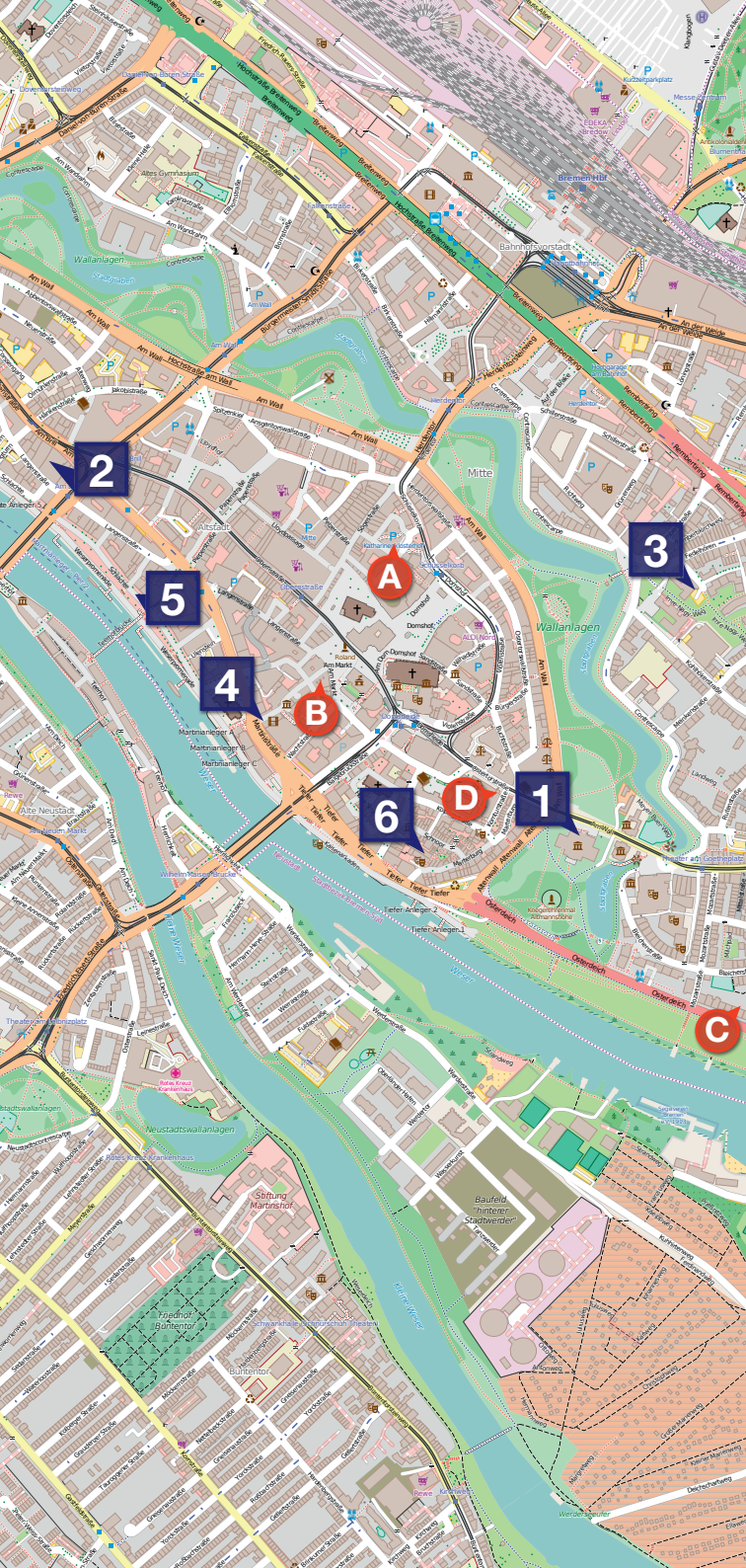
Discover Bremen

We do have a few suggestions how to make the most of your time in Bremen after the Congress:

Nearby, just down the street from Kunsthalle is the „Viertel“, a lively quarter with lots of atmosphere: many nice little restaurants and iconic pubs, extraordinary fashion from exclusive to second-hand. A vivid, sometimes slightly dirty part of Bremen, a cultural mile where latte macchiato meets canned beer.

Always a good choice: Schlachte, the Weser esplanade, is where Bremeners go to relax and treat themselves to an after-work drink or a good meal. Why not join them?

No matter what you decide to do, we are always keen on helping you to make the best out of your time in Bremen. Please just ask and we will be glad to assist you.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Martinianleger B
Martinianleger C
Tiefer
Tiefer Anleger 1
Tiefer Anleger 2
Osterdeich
Alte Neustadt
Bremen Hbf
Weser
Werdersee

Points of Interest:

1. Kunsthalle (conference hall)

2. Motel One

3. Ibis Hotel Remberti

4. Radisson Blu Hotel

5. Esplanade with Restaurants & Cafes

6. Schnoor (medieval quarter)

A. Wednesday Lunch
Stadtwirt

B. Thursday Lunch
Restaurant 1783

C. Thursday Banquet Dinner
Jürgenshof

D. Friday Lunch
Comturei

Access to the Wireless Internet

We provide WiFi for you, being guest of the VARI & PATMOS 2016. No additional software needs to be added to your notebook.

The password and further details will be povided at the Kunsthalle.

At a glance

Wednesday	
8:00–8:30	Registration
8:30–9:00	Welcome Note
9:00–10:00	Keynote – Prof. Asen Asenov
10:00–10:30	Coffee Break
10:30–13:00	PATMOS Session
13:00–14:30	Lunch
14:30–16:00	PATMOS Special Session
16:00–16:45	Coffee Break and Poster Session

Thursday	
8:30–9:30	Keynote - Prof. Christian Piguet
9:30–11:00	VARI Session
11:00–11:30	Coffee Break
11:30–12:30	Keynote - Prof. Tibor Grasser
12:30–14:00	Lunch
14:00–15:00	VARI Tutorial
15:00–16:20	PATMOS Session
16:20–17:00	Coffee Break and Poster Session
17:00–18:00	PATMOS Session
19:40	Meeting for Banquet Dinner / Jürgenshof

Friday	
8:30–10:00	PATMOS Session
10:00–10:30	Coffee Break
10:30–12:00	PATMOS Session
12:00–13:30	Lunch
13:30–16:30	PATMOS Session
16:30–17:20	PATMOS Special Session
17:20–18:00	Closing & Award Ceremony